IN THE CLAIMS

Claims 1-11 (canceled).

Claim 12. (New) An NROM memory cell structure formed on a substrate, the cell structure comprising:

one source and one drain regions formed inside the substrate;

one gate structure formed on the substrate between the source region and the drain region, the gate structure including an oxide-nitride-oxide layer and a control gate layer sequentially stacked on the substrate, wherein said gate structure has a waist portion wider than two ends thereof respectively adjacent to the source region and the drain region such that a source-side electron injection is minimized when a programming action is proceeded.

Claim 13. (New) The NROM memory cell structure of claim 12, wherein the waist portion is roughly at a symmetrical line that runs across the central region of the gate structure between the source and the drain regions.

Claim 14. (New) The NROM memory cell structure of claim 12, wherein in a programming operation, a portion of the gate structure close to the source region serves as an equivalent source region such that an overall size of the equivalent source region is greater than the drain region so as to prevent a second bit effect.

Claim 15. (New) The NROM memory cell structure of claim 12, wherein the gate structure is roughly a hexagonal shape with two sides being adjacent to the source and the drain regions.